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1 Performance bounds of partial run-time reconfiguration in high-performance reconfigurable computing
Esam El-Araby, Ivan Gonzalez, Tarek El-Ghazawi
November 2007 **HPRCTA '07:** Proceedings of the 1st international workshop on High-performance reconfigurable computing technology and applications: held in conjunction with SC07
Publisher: ACM Request Permissions
Full text available: Pdf (1.05 MB)
Bibliometrics: Downloads (6 Weeks): 10, Downloads (12 Months): 79, Downloads (Overall): 368, Citation Count:

High-Performance Reconfigurable Computing (HPRC) systems have always been characterized by their high performance and flexibility. Flexibility has been traditionally exploited through the Run-Time Reconfiguration (RTR) provided by most of the available ...

Keywords: dynamic partial reconfiguration, field programmable gate arrays (FPGA), high performance computing, reconfigurable computing

2 Incremental Placement for Timing Optimization
Wongoon Choi, Kia Bazargan
November 2003 **ICCAD '03:** Proceedings of the 2003 IEEE/ACM international conference on Computer-aided desig
Publisher: IEEE Computer Society
Full text available: Pdf (144.61 KB)
Bibliometrics: Downloads (6 Weeks): 0, Downloads (12 Months): 29, Downloads (Overall): 174, Citation Count: 1

An incremental timing driven placement algorithm is presented.We introduce a fast path-based analytical approach for timingimprovement. Our method achieves timing optimization byreducing the enclosing bounding boxes of selected nets oncritical paths. ...

3 An algorithm for mapping loops onto coarse-grained reconfigurable architectures
Jong-eun Lee, Kiyoung Choi, Nikil D. Dutt
July 2003 **LCTES '03:** Proceedings of the 2003 ACM SIGPLAN conference on Language, compiler, and tool for embedded systems
Publisher: ACM Request Permissions
Full text available: Pdf (78.69 KB)
Bibliometrics: Downloads (6 Weeks): 1, Downloads (12 Months): 22, Downloads (Overall): 244, Citation Count: 5

With the increasing demand for flexible yet highly efficient architecture platforms for media applications, there a growing interest in the Coarse-grained Reconfigurable Architectures (CRAs). While many CRAs have demonstrated impressive performance ...

Keywords: ALU array, coarse-grained reconfigurable architecture, mapping algorithm, memory bandwidth utilization

Also published in:
July 2003 **SIGPLAN Notices** Volume 38 Issue 7

4 Path sharing and predicate evaluation for high-performance XML filtering
Yanlei Diao, Mehmet Altinel, Michael J. Franklin, Hao Zhang, Peter Fischer
December 2003 **Transactions on Database Systems (TODS)** , Volume 28 Issue 4
Publisher: ACM Request Permissions
Full text available: Pdf (543.40 KB)
Bibliometrics: Downloads (6 Weeks): 6, Downloads (12 Months): 80, Downloads (Overall): 1652, Citation Count:

XML filtering systems aim to provide fast, on-the-fly matching of XML-encoded data to large numbers of query specifications containing constraints on both structure and content. It is now well accepted that approaches us event-based parsing and Finite ...

Keywords: Nondeterministic Finite Automaton, XML filtering, content-based matching, nested path expressio path sharing, predicate evaluation, structure matching

5 Algorithms for large-scale flat placement

Jens Vygen

June 1997 **DAC '97:** Proceedings of the 34th annual Design Automation Conference

Publisher: ACM  Request Permissions

Full text available: Pdf (1.99 MB)

Bibliometrics: Downloads (6 Weeks): 2, Downloads (12 Months): 24, Downloads (Overall): 324, Citation Count: 3

This is a survey on the algorithms which are part ofa program for flat placement of large-scale VLSI processorchips. The basis is a quadratic optimization approachcombined with a new quadrisection algorithm.In contrast to most previous quadratic placement ...

6 A grid-enabled MPI: message passing in heterogeneous distributed computing systems

Ian Foster, Nicholas T. Karonis

November 1998 **Supercomputing '98:** Proceedings of the 1998 ACM/IEEE conference on Supercomputing (CDRC

Publisher: IEEE Computer Society

Full text available: Html (52.16 KB)

Bibliometrics: Downloads (6 Weeks): 6, Downloads (12 Months): 57, Downloads (Overall): 879, Citation Count: 5

Application development for high-performance distributed computing systems, or computational grids as they sometimes called, requires ``grid-enabled'' tools that hide mundane aspects of the heterogeneous grid environment without compromising performance. ...

Keywords: MPI, MPICH, Message Passing Interface, computational grids, globus, metacomputing

7 TRAC: toward recency and consistency reporting in a database with distributed data sources

Jiansheng Huang, Jeffrey F. Naughton, Miron Livny

September 2006 **VLDB '06:** Proceedings of the 32nd international conference on Very large data bas

Publisher: VLDB Endowment

Full text available: Pdf (588.56 KB)

Bibliometrics: Downloads (6 Weeks): 1, Downloads (12 Months): 20, Downloads (Overall): 223, Citation Count: 1

Distributed computing environments, including workflows in computational grids, present challenges for monitoring, as the state of the system may be captured only in logs distributed throughout the system. One approach to monitoring such systems is to ...

8 Splitting interfaces: making trust between applications and operating systems configurable

Richard Ta-Min, Lionel Litty, David Lie

November 2006 **OSDI '06:** Proceedings of the 7th symposium on Operating systems design and implementation

Publisher: USENIX Association

Full text available: Pdf (387.24 KB)

Bibliometrics: Downloads (6 Weeks): 9, Downloads (12 Months): 35, Downloads (Overall): 178, Citation Count: 7

In current commodity systems, applications have no way of limiting their trust in the underlying operating sys (OS), leaving them at the complete mercy of an attacker who gains control over the OS. In this work, we describe the design and implementation ...

9 Verification of a Microcontroller IP Core for System-on-a-Chip Designs Using Low-Cost Prototyping Environments

Stephen Schmitt, Wolfgang Rosenstiel

February 2004 **DATE '04: Proceedings of the conference on Design, automation and test in Europe - Volume 3** , Volume 3

Publisher: IEEE Computer Society

Full text available: Pdf (281.80 KB)

Bibliometrics: Downloads (6 Weeks): 1, Downloads (12 Months): 24, Downloads (Overall): 134, Citation Count: 1

Rapid prototyping is a fast and efficient way for the functional verification of Systems-on-a-Chip in an early st of the design process. Because of the rising part of software in those systems the use and reuse of microcontroller IP cores is necessary ...

10 Layout aware optimization of high speed fixed coefficient FIR filters for FPGAs
Shahnam Mirzaei, Ryan Kastner, Anup Hosangadi
January 2010 **International Journal of Reconfigurable Computing** , Volume 2010
Publisher: Hindawi Publishing Corp.
Full text available: Pdf (1.30 MB)
Bibliometrics: Downloads (6 Weeks): 0, Downloads (12 Months): 0, Downloads (Overall): 0, Citation Count: 0

We present a method for implementing high speed finite impulse response (FIR) filters on field programmable gate arrays (FPGAs). Our algorithm is a multiplierless technique where fixed coefficient multipliers are replace with a series of add and shift ...

11 Sub-block subsampling based block-matching motion estimation
Reeba Korah, M. Sankarasingam, J. Raja Paul Perinbam
December 2004 **AIC'04:** Proceedings of the 4th WSEAS International Conference on Applied Informatics and Communications
Publisher: World Scientific and Engineering Academy and Society (WSEAS)
Bibliometrics: Downloads (6 Weeks): n/a, Downloads (12 Months): n/a, Downloads (Overall): n/a, Citation Count

Motion estimation has been widely employed in popular video standards like H.26x, MPEG - 1,-2 and - 4 to exploit the temporal redundancies inherent within image frames. Block matching is the most popular method f motion estimation. The disadvantages ...

Keywords: SSSAD, block matching, full search, motion estimation, sub-block, sub-sampling

12 Proceedings of the conference on Design, automation and test in Europe: Proceedings: Proceedings
Georges Gielen
March 2006 **DATE '06:** Proceedings of the conference on Design, automation and test in Europe: Proceedir
Publisher: European Design and Automation Association
Bibliometrics: Downloads (6 Weeks): n/a, Downloads (12 Months): n/a, Downloads (Overall): n/a, Citation Count

Welcome to the **DATE 06** Conference Proceedings. DATE combines the world's favourite electronic systems design conference and Europe's leading international exhibition for electronic design, automation and test. The *DATE 06 event* features ...

13 Energy-Aware Communication and Task Scheduling for Network-on-Chip Architectures under Real-Tim Constraints
Jingcao Hu, Radu Marculescu
February 2004 **DATE '04: Proceedings of the conference on Design, automation and test in Europe - Volume 1** , Volume 1
Publisher: IEEE Computer Society
Full text available: Pdf (154.78 KB)
Bibliometrics: Downloads (6 Weeks): 11, Downloads (12 Months): 110, Downloads (Overall): 413, Citation Count

In this paper, we present a novel Energy-Aware Scheduling (EAS) algorithm which statically schedules both communication transactions and computation tasks onto heterogeneousNetwork-on-Chip (NoC) architectures under real-time constraints. Our algorithm ...

14 A survey of fault tolerant methodologies for FPGAs
Jason A. Cheatham, John M. Emmert, Stan Baumgart
April 2006 **Transactions on Design Automation of Electronic Systems (TODAES)** , Volume 11 Issue 2
Publisher: ACM Request Permissions
Full text available: Pdf (932.02 KB)
Bibliometrics: Downloads (6 Weeks): 18, Downloads (12 Months): 142, Downloads (Overall): 899, Citation Count

A wide range of fault tolerance methods for FPGAs have been proposed. Approaches range from simple architectural redundancy to fully on-line adaptive implementations. The applications of these methods also dif some are used only for manufacturing ...

Keywords: FPGA, fault tolerance, self test

15 Partitioning graphs to speedup Dijkstra's algorithm

Rolf H. Möhring, Heiko Schilling, Birk Schütz, Dorothea Wagner, Thomas Willhalm

February 2007 **Journal of Experimental Algorithmics (JEA)** , Volume 11

Publisher: ACM Request Permissions

Full text available: Pdf (893.58 KB)

Bibliometrics: Downloads (6 Weeks): 19, Downloads (12 Months): 239, Downloads (Overall): 1434, Citation Cour

We study an acceleration method for point-to-point shortest-path computations in large and sparse directed graphs with given nonnegative arc weights. The acceleration method is called the *arc-flag approach* and is bas on Dijkstra's algorithm. ...

Keywords: Dijkstra's algorithm, Shortest path, acceleration method, road network

16 A hardware Memetic accelerator for VLSI circuit partitioning

Stephen Coe, Shawki Areibi, Medhat Moussa

July 2007 **Computers and Electrical Engineering** , Volume 33 Issue 4

Publisher: Pergamon Press, Inc.

Bibliometrics: Downloads (6 Weeks): n/a, Downloads (12 Months): n/a, Downloads (Overall): n/a, Citation Count

During the last decade, the complexity and size of circuits have been rapidly increasing, placing a stressing demand on industry for faster and more efficient CAD tools for VLSI circuit layout. One major problem is the computational requirements for ...

Keywords: Circuit partitioning, FPGA, Genetic algorithms, Handel-C, Hardware accelerator, Memetic algorithn

17 Virtual Hardware Byte Code as a Design Platform for Reconfigurable Embedded Systems

Sebastian Lange, Udo Kebschull

March 2003 **DATE '03: Proceedings of the conference on Design, Automation and Test in Europe - Volu 1** , Volume 1

Publisher: IEEE Computer Society

Full text available: Pdf (244.68 KB)

Bibliometrics: Downloads (6 Weeks): 1, Downloads (12 Months): 20, Downloads (Overall): 112, Citation Count: 1

Reconfigurable hardware will be used in many future embedded applications. Since most of these embedded systems will be temporarily or permanently connected to a network, the possibility to reload parts of the application at run time arises. In the 90ies ...

Keywords: Virtual Hardware Machine, Byte Code, FPGA

18 Perfecto: A systemc-based design-space exploration framework for dynamically reconfigurable architectures

Pao-Ann Hsiung, Chao-Sheng Lin, Chih-Feng Liao

September 2008 **Transactions on Reconfigurable Technology and Systems (TRETS)** , Volume 1 Issue 3

Publisher: ACM Request Permissions

Full text available: Pdf (3.72 MB)

Bibliometrics: Downloads (6 Weeks): 9, Downloads (12 Months): 93, Downloads (Overall): 395, Citation Count: 0

To cope with increasing demands for higher computational power and greater system flexibility, dynamically a partially reconfigurable logic has started to play an important role in embedded systems and systems-on-chip (SoC). However, when using traditional ...

Keywords: Reconfigurable systems, design-space exploration, partitioning, performance evaluation, placeme scheduling

19 Tornado: A self-reconfiguration control system for core-based multiprocessor CSoPCs

Armando Astarloa, Aitzol Zuloaga, Unai Bidarte, José Luis Martín, Jesús Lázaro, Jaime Jiménez
September 2007 **Journal of Systems Architecture: the EUROMICRO Journal** , Volume 53 Issue 9
Publisher: Elsevier North-Holland, Inc.

Bibliometrics: Downloads (6 Weeks): n/a, Downloads (12 Months): n/a, Downloads (Overall): n/a, Citation Count

In this work we present a self-reconfiguration control focused on multiprocessor core-based systems implemented on FPGA technology. An infrastructure of signals, protocols, interfaces and a controller is expose perform safe hardware/software reconfigurations. ...

Keywords: Dynamic reconfiguration, FPGA, Multiprocessor, Partial reconfiguration, SoC, SoPC

20 Gilgamesh: a multithreaded processor-in-memory architecture for petaflops computing
Thomas L. Sterling, Hans P. Zima
November 2002 **Supercomputing '02:** Proceedings of the 2002 ACM/IEEE conference on Supercompu
Publisher: IEEE Computer Society Press
Full text available: Pdf (322.86 KB)

Bibliometrics: Downloads (6 Weeks): 2, Downloads (12 Months): 35, Downloads (Overall): 519, Citation Count: 9

Processor-in-Memory (PIM) architectures avoid the von Neumann bottleneck in conventional machines by integrating high-density DRAM and CMOS logic on the same chip. Parallel systems based on this new technolo are expected to provide higher scalability, ...
Keywords: Petaflops computing, Processor-In-Memory, data parallel processing, irregular applications, parall architectures

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